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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

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Analogue self-calibration method and apparatus for low noise, fast and wide-locking range phase locked loop

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ANALOGUE SELF-CALIBRATION METHOD AND APPARATUS FOR LOW NOISE, FAST AND WIDE-LOCKING RANGE PHASE LOCKED LOOP

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a Phase Locked Loop (PLL) circuit having a variable output frequency. More particularly, the present invention consists of an improved method for a fast and automatic setting of the output frequency of PLL synthesizers that overcomes the classical problems associated with prior implementation, concerning: linearity, locking range limitation, settling time, jitter, phase noise, and spectral purity deterioration.

Description of the Prior Art

A Phase-Locked Loop (PLL) synthesizer is a circuit used to generate a periodic signal with a precise frequency. This kind of circuits is widely used in many communication and measurement products. Its application includes also advanced digital systems, such as microprocessors and micro-controllers. The PLL circuits should be designed with stringent constraints in term of noise performances, settling time, power consumption, locking range, integration, cost, etc.

Typically PLLs include a phase detector that compares the phase of the reference signal to the phase of an internal feedback signal, a charge pump and a low pass loop filter for setting an analogue voltage proportional to the detected phase difference, a Voltage-Controlled Oscillator (VCO) that generate a periodic output signal with a frequency proportional to its input voltage, and a frequency divider that generates the feedback signal after dividing the frequency of the output signal by a predefined integer or fractional number (N).

Two seemingly contradictory requirements constitute the fundamental forces driving the design of VCOs: On one hand, a wide frequency tuning range and thus a high VCO gain are needed to compensate temperature and process variation and to cover the frequency band of the considered application. At the same time, the gain of the VCO should be as small as possible to meet phase noise and spectral purity specifications. In fact, the more VCO has a high gain the more its sensitivity to the

noise in its control path increases. The VCO control path is in general affected by several noise sources that include: charge pump noise, filter noise and ripple due to mismatching between the charge pump up and down currents. The noise in the signal path generated by the active elements of the VCO is also dramatically amplified and converted to the phase noise if the VCO gain is high.

Some approaches for simultaneously reducing the VCO gain and enabling a wide frequency range were recently presented as for example in US5942949 patent document. All these solutions consist in breaking the wide range tuning curve into several narrower-range sections with some frequency overlap. A digital calibration of a switched-capacitor network is used to choose the appropriate narrow-range section before starting an analogue fine frequency tuning over this curve.

Additional blocks are needed to build a second loop, which achieves the digital self-calibration of the VCO. The second loop is generally constituted by a phase/frequency detector, a charge pump followed by a capacitor or a digital accumulator, and a state machine that applies a sequence of digital control inputs values to the VCO. The complexity of those extra blocks increases proportionally to the needed accuracy of the output frequency. Moreover, since the consecutive digital control words (e.g. 11110 and 00001) can use totally different units of the switched-capacitor network, the accumulated capacitance errors due to process variation can reach very high values (even several time the value of the switched-capacitor network unit in the case of a 5 bits control). Therefore, a very high frequency overlap is required to compensate these errors, leading to a higher gain of the VCO, a lower total tuning range, and a higher parasitic capacitance. This is why digital calibration can result in prolonged design cycles with a significant additional area and cost of the system.

This digital self-calibration is in general implemented with a simple algorithm such as sequential search as well as with more complex ones such as binary search. However, the time needed for those searching algorithms is often so high that only a self-calibration during the power up of the system is possible. Many side effects can affect the PLL output frequency during its on-mode such as temperature variation, power supply fluctuation, injection pulling etc. Therefore if the frequency varies significantly during the on-mode of the system, the PLL will not be able to correct this

variation within a reasonable time. Moreover, The PLL settling time is one of the most important criteria for many applications. It is even the most critical figure for systems dedicated to fast frequency-hopped spread-spectrum, Ultra-Wideband or data recovery. Therefore, it would be desirable to simultaneously reduce VCO gain and enable a wide frequency tuning range, without using the time consuming digital self-calibration.

SUMMARY OF THE INVENTION

The aim of the present invention is to provide a method and apparatus for a fast and automatic setting of the phase locked loop (PLL) output frequency over a wide tuning range, with a very low VCO gain during the in-lock state to improve the noise performances, and without using the costly, complex and time consuming digital self-calibration techniques.

This aim is achieved with a Method for analogue self-calibrating of a phase locked loop circuit comprising a phase frequency detector, a charge pump, a loop filter, a voltage controlled oscillator, including a plurality of VCO tuned elements, which output signal is compared with a reference signal frequency entering in the phase frequency detector characterized in that, the voltage controlled oscillator operating mode, using a linearized frequency versus voltage curve, is switched, in a first frequency tuning operation, to a linear high gain mode, enabling a fast and a wide tuning range, after locking to the appropriate frequency with the said first tuning operation, said voltage controlled oscillator operating mode is automatically switched to a zero-gain mode while keeping the frequency of said voltage controlled oscillator unchanged, the sensitivity of the said voltage controlled oscillator to the noise in the control path is then practically eliminated and the phase noise performances significantly improved, and optionally, after said zero-gain mode, said voltage controlled oscillator operating mode is switched to a low gain mode enabling a fine tuning of the frequency by the phase locked loop for compensating small residual frequency errors and temperature variations.

The present invention concerns also an Integrated circuit comprising a phase locked loop circuit including, a phase or frequency detector that compares the phase and frequency of a reference signal to the phase and frequency of an internal feedback

signal and generates output error signals, a charge pump that generates amounts of charges proportional to said output error signals, a loop filter for setting an analogue voltage proportional to the charges accumulated in their capacitors, characterized in that said phase locked loop circuit includes a voltage-controlled oscillator with multiples inputs corresponding each to a VCO tuned element, working in a linear high-gain mode and generates a periodic output signal with a frequency proportional to the voltage supplied by the loop filter and a circuit providing a linear variation of the voltage-controlled oscillator frequency over the voltage tuning range, comprising offsets generators circuits that generate the voltages applied to the multiples inputs of the voltage-controlled oscillator after shifting the loop filter output voltage with predefined offsets.

A VCO tuned element corresponds here either to a varactor (voltage controlled capacitor) to a voltage controlled current sources VCI or to any other voltage controlled component varying the frequency of the VCO. A set of these elements respectively constitutes a voltage-controlled oscillator VCO provided with several inputs as described below.

In general the present invention is a PLL-based frequency synthesizer having a reconfigurable VCO with three modes of operation: a Linear-High-gain, Zero-gain, and Low-gain mode. During a first tuning operation, a Gain-Mode Switcher sets the VCO in a high gain mode, enabling wide-locking range of the synthesizer with a fast settling time. During this operation, the control voltage of the VCO is varied by the PLL until the appropriate output frequency is found.

When the loop is locked, the VCO is automatically switched to Zero-gain mode by the Gain-Mode Switcher, while keeping the frequency of its output signal practically constant. Its sensitivity to the noise in the control path is then practically eliminated and its phase noise performances significantly improved. If the frequency error is sufficiently small for the considered application, the tuning is stopped at this stage. If the error is not sufficiently small the VCO is switched again to Low-gain mode and fine-tuning adjustment of the output frequency is achieved.

Another embodiment of the present invention is a method and apparatus for providing a linear variation of the frequency over all the voltage tuning range. The

application of this method is particularly important during the High-gain mode, where the VCO gain variation may leads to serious degradation of the loop stability margin and the noise performances.

The present invention is not limited to charge-pump PLLs. As long as the circuit has a tuning system using a variable capacitance or a variable current, the reconfigurable three-mode (Linear-High-gain, Zero-gain, and eventually Low-gain) varactor (voltage controlled capacitor) or controlled current source using a Gain-Mode Switcher in accordance with the present invention, can be used for setting the desired value of the capacitance or the current.

BRIEF DESCRIPTION OF THE DRAWINGS

It is noted that the appended drawings illustrate only exemplary embodiments of the invention and are, therefore, not considered limiting of its scope.

FIG. 1 illustrates a block diagram of a charge-pump phase locked loop system in accordance with the present invention;

FIG. 2 diagrammatically shows the Gain-Mode Switcher incorporated into the PLL of FIG. 1;

FIG. 3 diagrammatically shows an exemplary implementation of an offset-generator unit (e.g. 201) of the gain-mode switcher of FIG. 2;

FIG. 4 diagrammatically shows an exemplary implementation of a switcher-comparator unit (e.g. 221) of the gain-switcher of FIG. 2;

FIG. 5 illustrates an exemplary embodiment of a multi-inputs-VCO and their controlled elements in accordance with the present invention and which can be incorporated in the PLL of FIG. 1;

FIG. 6 illustrates another exemplary embodiment of a multi-inputs-VCO and their controlled elements in accordance with the present invention and which can be incorporated in the PLL of FIG. 1;

FIG. 7 shows a hypothetical frequency versus voltage characteristic needed for the considered application;

FIG. 8 the curve 820 shows a hypothetical capacitance versus voltage characteristic needed for the considered application, and C01 to C19 curves show the capacitance versus voltage curves used to build the curve. 1;

FIG. 9 curves V01 to V19 illustrate the output voltages of the offset generators implemented in the gain-mode switcher of FIG. 2. These output voltages are applied to the capacitors units 501 to 519 of the multi-inputs-VCO of FIG. 5;

FIG. 10 illustrates the input 1003 and output 1002 voltage of the comparator 405 illustrated in FIG. 4;

FIG. 11 illustrates the capacitance versus control voltage characteristics of the VCO, during linear-high-gain mode curve 820, zero-gain mode curve 1101, and low-gain mode curve 1102;

FIG. 12 diagrammatically shows the pattern of some internal signals of the PLL system of FIG. 1, and exemplary variations of control voltage (1201, 1202, 1203) during the loop settlings.

DETAILED DESCRIPTION

FIG.1 is a functional block diagram of the charge pump phase locked loop (PLL) system in accordance with the present invention. The PLL circuit, generally designed 100, includes a Phase/Frequency detector (PFD) 121 to compares the phase and the frequency of the reference signal (Fref) to the phase and the frequency of the feedback signal 128, and generates an error signal. The error signal is either an up signal or a down signal depending on the sign of the detected error.

Charge pump CP 122 generates an amount of charge equivalent to the error signal provided by the Phase/Frequency detector PFD 121. Depending upon the polarity of the signal (up or down), the charge is either added to or subtracted from a capacitor in the Low Pass Filter (LPF) 123. Accordingly, the low pass loop filter 123 generates a voltage 124 that will be applied to the input of the Gain-Mode Switcher 125 (GMS).

The Gain-Mode Switcher (GMS) 125 is the block of the PLL 100 that enables to change the gain mode of the VCO 126 during the tuning operations. Three operation modes are possible: A Linear-High-Gain mode (LHG-mode), Zero-Gain mode (ZG-

mode), and Low-Gain mode (LG-mode). The Gain-Mode Switcher (GMS) 125 is composed on N parallel paths. N is equal to 19 in the exemplary Gain-Mode Switcher embodiment of FIG. 2. Each path includes an Offsets-Generator OG (e.g., 201) and a Switcher-Comparator SC (e.g., 221).

Each Offset-Generator OG (e.g., 201) receives the voltage V_t 124 at its input and generates an output voltage with an added offset, that is $V_t + \Delta V$ (e.g., 243). The values of the generated offsets will be varied from one Offset-Generator OG to the other by varying the dimensions of their components. FIG. 3 illustrates an exemplary embodiment of the Offset-Generator OG incorporated in Gain-Mode Switcher (GMS) 125. The dimensions $(W/L)_1$ and $(W/L)_2$ of transistors 301 and 302 are chosen in such way that $(W/L)_2$ is equal to k x $(W/L)_1$. By changing the value of k, one can change the value of the offset ΔV. The parameter k will be chosen either higher than 1 or lower than 1. The Offset-Generators OG with k higher than 1 will generate a positive offset and those with k lower than 1 will generate a negative offset. The output voltage of each Offset-Generator OG (e.g., 201) is applied to a Switcher-Comparator SC (e.g., 221).

Fig. 4 shows an exemplary embodiment of a Switcher-Comparator SC unit of the Gain-Mode Switcher (GMS) 125. In the first tuning, the PLL is started in LHG-mode, each Switcher-Comparator SC (e.g., 221) of the Gain-Mode Switcher (GMS) 125 will enable to apply its input voltage $V_t + \Delta V$ (e.g., 243) directly to one of the inputs of the VCO (e.g., 101). After a first locking, the input voltage $V_t + \Delta V$ of each Switcher-Comparator SC will be compared to Vref 406, and its output switched to zero or to the power supply voltage Vcc depending upon the $V_t + \Delta V$ is higher or lower than Vref. In this example, Vref corresponds to the middle of the capacitance versus voltage characteristic of the used varactors (among 501 to 519). The capacitance of these varactors is thus switched to its maximum Cmax or to its minimum Cmin, depending upon its value was at Cmax or at Cmin when the PLL was locked at the end of the LHG-mode. By this operation the mode is switched to ZG-mode while keeping the total capacitance and so the output frequency unchanged.

The present invention can be applied on two types of PLL configuration:

a) The PLL with a capacitance controlled VCO, such as Inductance – capacitance LC oscillator, which is driven by a voltage varying a set of capacitances (varactors). This PLL is often used in radio-frequency (RF) applications for large frequency ranges. The main advantage of LC VCO is its low phase noise.

FIG. 5 shows an exemplary of the multi-inputs VCO incorporated in FIG. 1. This schematic is an embodiment of a modified inductance L - capacitance C VCO (LC VCO), which has several variable capacitors (e.g., 501 to 520 in FIG. 5). The values of these capacitors units 501 to 520 are controlled by input voltages 101-120 supplied by the Gain-Mode Switcher (GMS) 125. The output frequency of the VCO depends on both the value of the inductance 521 and the value of the capacitors 501 to 520. The active circuit AC 522 generates the required negative impedance for the circuit to oscillate.

b) The ring oscillator PLL, which is driven by a voltage varying a set of current sources. This PLL is preferably used in digital applications and/or at low frequency ranges. The main advantage is this type of PLL is its compactness and wide tuning range performance.

FIG. 6 shows an example of VCO using voltage controlled current sources (VCI) that can be incorporated in FIG. 1 to replace the LC VCO as shown in FIG. 5. The voltage controlled oscillator VCO is made by a current controlled oscillator ICO preceded by voltage - current V-I converters at each input. The values of the currents 601 to 620 generated by the converters are controlled by input voltages 101-120 supplied by the Gain Mode Switcher (GMS) 125. The output frequency of the oscillator depends then on the values of the currents 601 to 620. The ring oscillator 621 can be implemented with a cascade of differential buffer delay stages as well as with an odd number of inverters.

The present invention will be clarified with the help of the hypothetical application illustrated in FIG. 7. PLL's are often designed for a wide range of frequencies. The wide frequency tuning range is needed to compensate temperature and process variation and to cover the frequency band of the considered application. In the case of the application illustrated in Fig. 7, a frequency tuning range of 800 MHz is needed. The PLL should be able to set any frequency in the band 1 GHZ to 1.8 GHz.

The available tuning voltage is about 2 V (i.e., from 0.5 V to 2.5 V), thus, the needed VCO gain (K_{VCO}) is 400 MHz/V. It is well known that the operating curves (i.e., input voltage versus output frequency) of classical VCOs are in general highly non-linear. A variation of the gain K_{VCO} will change the open-loop gain and hence change the loop bandwidth and phase margin. This is why in this hypothetical application of FIG. 7 a linear operating curve with a constant K_{VCO} is targeted.

The curve 820 of FIG.8 illustrates the needed capacitance versus voltage characteristic of the VCO varactor to produce the operating curve 701. 820 is deduced from 701 by using the well-known formula $2\pi F = (LC)^{-1/2}$, where F is the frequency of the VCO output signal, and L and C are respectively the equivalent parallel inductance (521) and capacitance (501-520) of the tank. To simplify the analysis, the fixed capacitance of the VCO is supposed to be negligible and its inductance 521 constant and equal to 2 nH. To built the wide-range curve 820, we start by breaking it into several narrower-range sections, 801 to 819. Each narrower-range section (e.g, 801) will be represented by an individual curve (e.g., C_{01}) having the same variation over the corresponding voltage interval (e.g., 0.1V in FIG. 8). As result, the curve 820 can be reconstituted entirely by a simple addition of the individual curves C_{01} to C_{19}. Each one of the curves C_{01} to C_{19} will correspond to a given varactor among the varactors 501 to 519 of FIG. 5.

The exemplary varactors 501 to 519 are MOS (Metal Oxide Semi-conductor) transistors, dimensioned in such way that there capacitance characteristics has respectively the same variation of C_{01} to C_{19}. In the exemplary embodiments of FIG. 5 the control voltage 124 is applied to the MOS capacitors 515 and generates the operating curve C_{15}. To generate the other operating curves $C_{15\pm i}$, that is C_{01} to C_{15} curves, a tuning voltage with a various offsets are applied to the corresponding MOS capacitors. More precisely, to generate the curve $C_{15\pm i}$, a voltage $V_{15\pm i} = V_t \pm 0.1 \times i$ will be applied to the corresponding MOS capacitor. This voltage is one among the voltages V_{01} to V_{19} illustrated in FIG. 9, which illustrate the output voltages of the offset generators implemented in the gain-mode switcher Gain-Mode Switcher (GMS) 125 of FIG. 2. Therefore when those output voltages are directly applied to the MOS capacitors 501 to 519 of the multi-inputs VCO of FIG. 5, the PLL works in

the LHG-mode and the resulting frequency versus tuning voltage curve is exactly the desired curve 701 of FIG. 7.

FIG. 12 diagrammatically shows the pattern of some internal signals of the PLL system 100, and exemplary variations of control voltage during the three modes of operations.

During a first tuning operation, the Gain-Mode Switcher (GMS) 125 sets the Multi-Inputs VCO 126 in the LHG-mode 1201. During this operation, switch 240 is open and 241 closed. Accordingly, the constant voltage V_{dc} 220, is provided to varactor 520, freezing its capacitance in the middle of its capacitance versus voltage characteristic. On the other hand, switch 401 of each Switcher-Comparator SC (among 221-239) of the Gain-Mode Switcher (GMS) is closed while 402, 403, 404 are open. Accordingly, the outputs voltages of the Offsets-Generators OG 201-219 are directly provided to varactors 501 to 519. The phase frequency detector PFD 121 and the charge pump CP 122 will vary the control voltage 124 and thus, through the Offset-Generators OG 201-219, will also vary the voltages 201-219 according to the curves V_{01}-V_{19} of Fig.9. During this tuning operation, the frequency is varied according to the wide-range curve 701 until the appropriate value is found. In the given example V_t 124 will be set to 1.5V (702) and output frequency to 1.42 GHz (703). The noise performance of the PLL is not critical at this stage. Therefore, in this mode the PLL can be optimized to be stable and have a fast settling time even if it will be at the cost of more noise. For this, a fraction of the filter capacitances can be optionally switched off and/or the current of the charge pump increased.

The duration of the LHG-mode 1201 is controlled by a Lock Detector LD 129. This mode is selected during a sufficiently long time for the loop to lock. When the control voltage 124 will converge to the needed value (e.g., 1.5 V 702), the Lock Detector LD send a signal to the Gain-Mode Switcher (GMS) and the VCO is switched to Zero-gain mode (ZG-mode in FIG. 12) by the Gain-Mode Switcher (GMS) 125, while keeping its frequency constant.

During the ZG-mode 1202 step, the switch 401 of each Switcher-Comparator SC among 221 to 239 is open, isolating the varactors 501-519 from the output voltages V_{01}-V_{19} of Offset-Generators (OG) 201-219. At the same time switch 403 and 402 are

closed. Voltages V_{01}-V_{19} will thus be compared to Vref 406 by the comparator 405. Vref 406, is chosen to correspond to the middle of the capacitance versus voltage characteristic C15 of FIG. 8, which corresponds to varactor 515 (e.g., Vref » 0.95 V). The output of 405 will then be switched to zero or to Vcc depending upon the input voltage is higher or lower than Vref. Accordingly, the capacitance of the varactors 501-519 will be switched to its maximum value or to its minimum value. To freeze the situation and to make it independent on future variations of the control voltage 124, switch 402 is opened and 404 is closed. The capacitance of the thank 501-519 are thus frozen and correspond to a constant capacitance (e.g., operating curve 1101), which is independent on Vt 124. The sensitivity to the noise in the control path is then practically eliminated and the phase noise performances of the PLL 100, significantly improved. At this stage, the equivalent output frequency of the VCO is equal to the desired frequency (e.g., 1.42 GHz 703) with a small error. The error can be reduced by increasing the number of fractions in FIG. 8 and thus increasing the number of VCO varactors in FIG. 5. If the frequency error is sufficiently small for the considered application the tuning is stopped.

If the error is not sufficiently small the VCO is switched to Low-Gain (LG) mode 1203. Switch 241 is opened and switch 240 is closed. The tuning voltage 124 is than applied to an additional varactor 520, and fine-tuning adjustment over operating curve 1102 is achieved.

Optionally, comparators are added to the Gain-Mode Switcher (GMS) 125 to set an upper and a lower limit for its input signal 124. Accordingly, these comparators will control the value of the signal 124. If during LG-mode 1203, this signal reaches either of the upper limit 1104 or the lower limit 1103, a Gain-Mode Switcher (GMS) 125 will be restarted, and LHG-mode 1201 is selected again. The limits are preferably set near Vcc for the upper (1104) and near zero for the lower (1103). This operation is useful if the fine-tuning range is not sufficiently wide to compensate frequency variation that can arise during LG-mode 1203. This frequency variation can be caused by a rise in the chip temperature for instance.

To preserve the stability of the PLL in both LHG-mode and LG-mode, the product of the charge pump CP 122 current and the gain of the VCO 126 will be kept constant. Therefore, a fraction of the charge pump CP current will be switched off during LHG-

mode 1201 and switched on during LG-mode 1203. Optionally, a fraction of the filter capacitance is switched off during LHG-mode 1201, resulting in significant improvement of the PLL settling time at the cost of a worst noise performance. In fact, the noise performance becomes critical only in the final LG-mode.

Another option particularly suitable for low voltage applications is to add a voltage doubler circuit that increase the voltage supply of the charge pump (CP), the loop filter and the offsets generators (OG) during the linear high-gain mode (LHG) and hence enhance the tuning range of the PLL. A switch configuration enabling the isolation of the noisy voltage doubler during the low gain (LG) mode and the application instead, the low noise output operating voltage supply is optionally added to save PLL spectrum purity.

CLAIMS

1. Method for analogue self calibrating of a phase locked loop (PLL) circuit comprising a phase frequency detector (PFD), a charge pump (CP), a loop filter (LPF), a voltage controlled oscillator (VCO), including a plurality of VCO tuned elements, which output signal is compared with a reference signal frequency (F_{ref}) entering in the phase frequency detector (PFD) characterized in that, the voltage controlled oscillator (VCO) operating mode, using a linearized frequency versus voltage curve, is switched, in a first frequency tuning operation enabling a wide locking range, to a linear high gain (LHG) mode, after locking to the appropriate frequency with the said first tuning operation, said voltage controlled oscillator (VCO) operating mode is automatically switched to a zero-gain (ZG) mode while keeping the frequency of said voltage controlled oscillator (VCO) unchanged and optionally, after said zero-gain (ZG) mode, said voltage controlled oscillator (VCO) operating mode is switched to a low gain (LG) mode enabling a fine tuning of the frequency by the phase locked loop (PLL) for compensating small residual frequency errors and temperature variations.

2. Method according to claim 1 characterized in that, the voltage controlled oscillator (VCO) frequency versus voltage operating curve linearization comprises following steps:

- breaking the required linear frequency versus voltage curve FV into several sections fV over either constant or non constant voltage intervals;
- selecting for each section fV a corresponding VCO tuned element giving the same frequency variation over said section fV;
- submitting each VCO tuned element to a specific voltage, deduced from the loop filter (LPF) output tuning voltage by adding a specific offset, in such way that said VCO tuned element is activated in the same voltage interval as its corresponding section fV.

3. Method according to claim 1 and 2 characterized in that the linearization of the voltage controlled oscillator (VCO) frequency versus voltage operating curve is performed during the linear-high gain (LHG) mode.

4. Method according to claim 1 characterized in that switching of the voltage controlled oscillator (VCO) from the linear-high-gain (LHG) mode to the zero-gain (ZG) mode comprises following steps:

- isolating the VCO tuned elements from their controlling voltages when the phase locked loop PLL is locked;
- comparing each VCO tuned element voltage to a reference voltage to determine if the value of said VCO tuned element was at it maximum or its minimum when the phase locked loop PLL is locked;
- depending on the result of this comparison, applying a voltage equal to zero or to the power supply voltage Vcc to each VCO tuned element switching its value to its maximum or to its minimum, the total value of said VCO tuned elements is thus equal to their value when the phase locked loop PLL was locked;
- freezing the VCO tuned elements in the state previously obtained by isolating them from the tuning voltage to activate thus the zero-gain (ZG) mode for the voltage controlled oscillator (VCO).

5. Method according to claim 1 characterized in that switching of the voltage controlled oscillator (VCO) from the zero-gain (ZG) mode to the low-gain (LG) mode comprises following steps:

- using an additional VCO tuned element that is dimensioned to achieve the needed fine tuning with a low voltage controlled oscillator (VCO) gain;
- linking said VCO tuned element to a fixed voltage during linear-high-gain (LHG) mode and zero-gain (ZG) mode;
- isolating said additional VCO tuned element from this fixed voltage during the switching step from zero-gain (ZG) mode to low-gain (LG) mode;
- linking said additional VCO tuned element to the tuning voltage supplied by the loop filter (LPF) of the phase locked loop PLL;
- achieving the fine tuning operation by the phase locked loop PLL.

6. Method according to claim 1 characterized in that the loop filter (LPF) output voltage is compared to an upper and a lower limit by means of additional comparators during low gain (LG) mode; the tuning operations are restarted and the initial linear high gain (LHG) mode is selected again when the loop filter (LPF) output voltage reaches either of the upper limit or the lower limit.

7. Method according to claim 1 characterized in that the phase locked loop PLL locking time during the linear high gain (LHG) mode is improved by switching off a fraction of the capacitance of the loop filter (LPF) or optionally by increasing the current of the charge pump (CP).

8. Method according to claim 1 characterized in that the phase locked loop PLL stability during the operations at the linear high gain (LHG) and the low gain (LG) modes is preserved by decreasing the charge pump (CP) current during the linear high gain mode (LHG) mode and by increasing said current during the low gain (LG) mode in such way that the product of the charge pump (CP) current and the gain of the voltage controlled oscillator (VCO) remains constant.

9. Integrated circuit comprising a phase locked loop (PLL) circuit including, a phase or frequency detector (PFD) that compares the phase and frequency (F_{ref}) of a reference signal to the phase and frequency of an internal feedback signal and generates output error signals, a charge pump (CP) that generates amounts of charges proportional to said output error signals, a loop filter (LPF) for setting an analogue voltage proportional to the charges accumulated in their capacitors,

characterized in that said phase locked loop (PLL) circuit includes a voltage-controlled oscillator (VCO) with multiples inputs corresponding each to a VCO tuned element, working in a linear high-gain (LHG) mode and generates a periodic output signal with a frequency proportional to the voltage supplied by the loop filter (LPF) and a circuit providing a linear variation of the voltage-controlled oscillator (VCO) frequency over the voltage tuning range, comprising offsets generators (OG) circuits that generate the voltages applied to the multiples inputs of the voltage-controlled oscillator (VCO) after shifting the loop filter (LPF) output voltage with predefined offsets.

10 Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 9 characterized in that the VCO tuned elements of the voltage controlled oscillator (VCO) include varactors dimensioned in such a way that the voltage controlled oscillator (VCO) has a constant voltage to frequency gain during the linear high gain (LHG) mode step, each varactor being controlled by a corresponding input of the voltage-controlled oscillator (VCO).

11. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 10 characterized in that the voltage-controlled oscillator (VCO) further comprises, an additional varactor that enables to achieve a fine frequency tuning during the low gain (LG) mode and a switch configuration enabling the application of a constant voltage to said varactor during the linear high gain (LHG) mode and the zero gain (ZG) mode, and the application of the loop filter (LPF) output voltage to said varactor during the low gain (LG) mode.

12. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 9 characterized in that the voltage controlled oscillator (VCO) is constituted by a current controlled oscillator (ICO) which include VCO tuned elements comprising voltage to current converters (V-I) including voltage controlled current sources (VCI) dimensioned in such way that the current controlled oscillator (ICO) has a constant voltage to frequency gain during the linear high gain (LHG) mode step, each controlled current sources (VCI) being controlled by a corresponding input of the voltage-controlled oscillator (VCO).

13. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 12 characterized in that each VCO tuned element further comprises, an additional controlled current sources (VCI) that enables to achieve a fine frequency tuning during the low gain (LG) mode and a switch configuration enabling the application of a constant voltage to said controlled current sources (VCI) during the linear high gain (LHG) mode and the zero gain (ZG) mode, and the application of the loop filter (LPF) output voltage to said controlled source (VCI) during the low gain (LG) mode.

14. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 9 characterized in that it further comprises a gain mode switcher (GMS) circuit connected between the loop filter (LPF) output and the voltage-controlled oscillator (VCO) inputs including comparators (SC) that compare the inputs voltage-controlled oscillator (VCO) voltages to a reference voltage, and according to the results of those comparisons, switch their output to a maximum value or to a minimum value; a switch configuration enabling the application of the voltages of offset generators (OG) to the inputs of the voltage-controlled oscillator (VCO) during the linear high gain (LHG) mode; during the transition to zero gain (ZG) mode the inputs are isolated

from the offset generators (OG), the output voltages of said offsets generators (OG) are applied to the inputs of the comparators (SC), the outputs voltages of said comparators (SC) are applied to the inputs of the voltage-controlled oscillator (VCO), and finally the state of each comparator (SC) is frozen and thus made independent on the loop filter (LPF) output voltage.

15. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 9 characterized in that it further comprises a lock detector (LD) that activates the switch configuration in such way that: the linear high gain (LHG) mode is selected during a sufficiently long time for the loop to lock and the transition to zero gain (ZG) mode is activated after this locking.

16. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 14 characterized in that it further comprises comparators that set an upper and a lower limit for the loop filter (LPF) output voltage during the low gain (LG) mode and restart the initial linear high gain (LHG) mode when said loop filter output voltage reaches either of these two limits.

17. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 9 characterized in that it further comprises a voltage doubler circuit that increase the voltage supply of the charge pump (CP), the loop filter (LPF) and the offsets generators (OG) during the linear high-gain mode (LHG) and hence enhance the tuning range of the PLL.

18. Integrated circuit comprising a phase locked loop (PLL) circuit according to claim 17 characterized in that it further comprises a switch configuration enabling the application of the voltage doubler to the charge pump (CP), the loop filter and the offsets generators (OG) during the linear high-gain mode (LHG) and the output operating voltage supply during the low gain (LG) mode.

ABSTRACT

A method and apparatus for a fast and automatic setting of the phase locked loop (PLL) output frequency that significantly improves linearity, locking range as well as spectrum purity, jitter and phase noise performances is disclosed. In one embodiment, a PLL frequency synthesizer is disclosed having a reconfigurable voltage controlled oscillator VCO with three modes of operation: a Linear-High-gain, Zero-gain, and Low-gain mode. During a first tuning operation, the VCO work in a linear high gain mode, enabling a totally analogue self-calibration of the PLL over a wide frequency tuning range and with a fast settling time. During this operation the control voltage at the input of the VCO is varied by the PLL until the appropriate output frequency is found. A method for providing a linear variation of the frequency over all the voltage tuning range during this mode is disclosed. When the loop is locked, the VCO is automatically switched to the Zero-gain mode while keeping its frequency unchanged. Its sensitivity to the noise in the control path is then practically eliminated and its phase noise performances significantly improved. If the frequency error and phase noise are sufficiently small for the considered application the tuning is stopped. If the error and phase noise are not sufficiently small the VCO is switched again to Low-gain mode and fine-tuning adjustment of the output frequency is achieved.

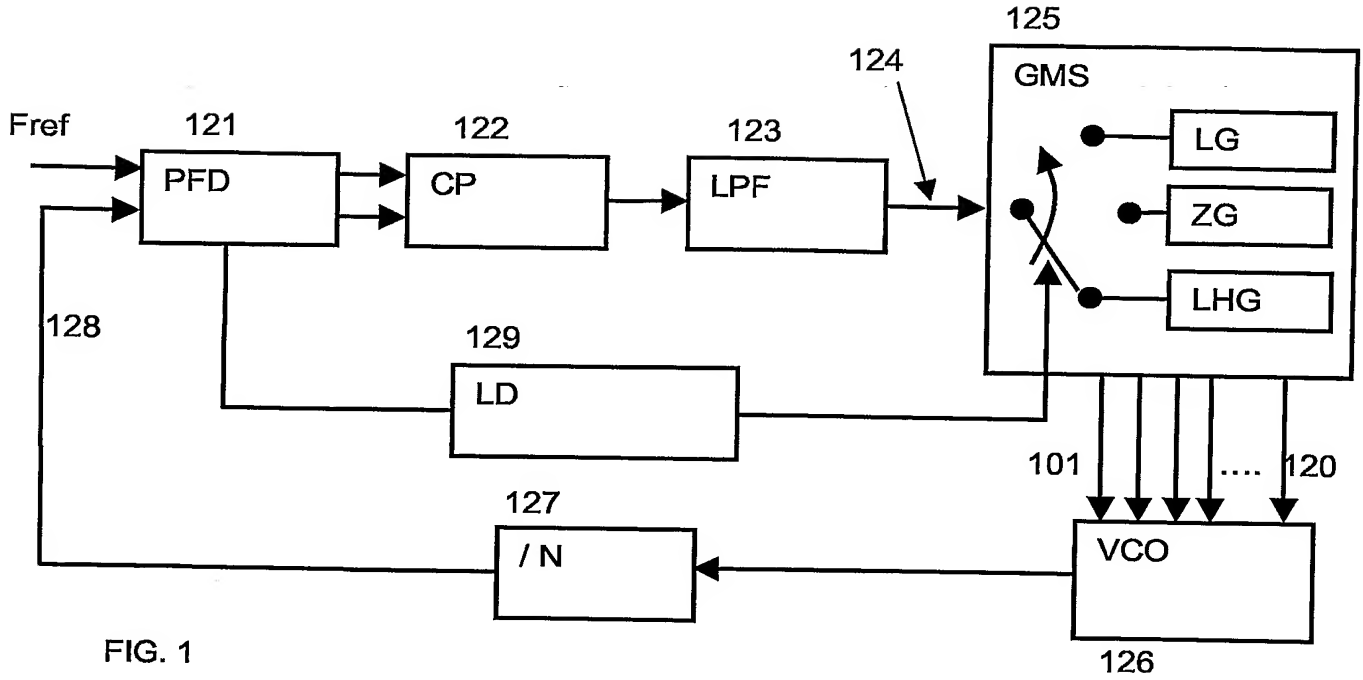
125
GMS
124
Fref
121
PFD
122
CP
123
LPF
LG
ZG
LHG
128
129
LD
101
....
120
127
/ N
VCO
126

FIG. 1

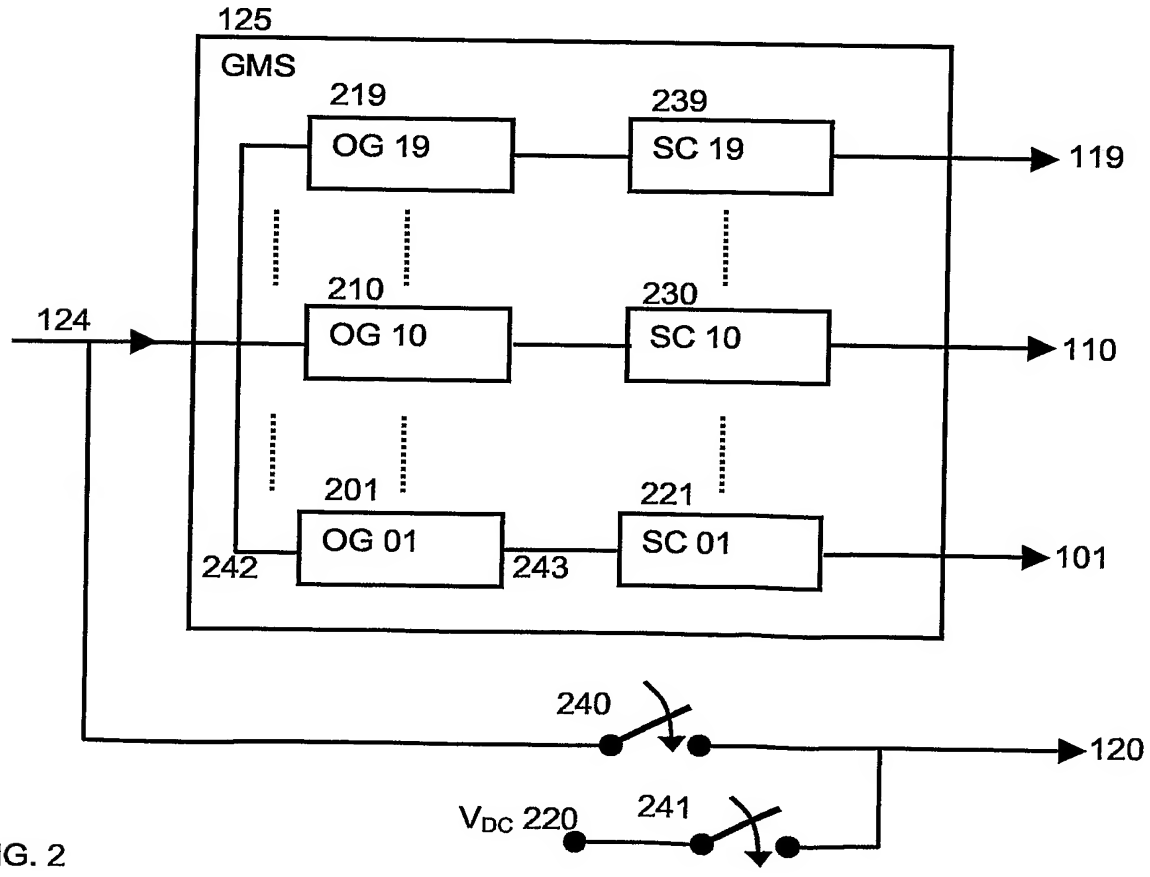
125
GMS
219
OG 19
239
SC 19
119
210
OG 10
230
SC 10
124
110
201
OG 01
221
SC 01
242
243
101
240
120
V_{DC} 220
241

FIG. 2

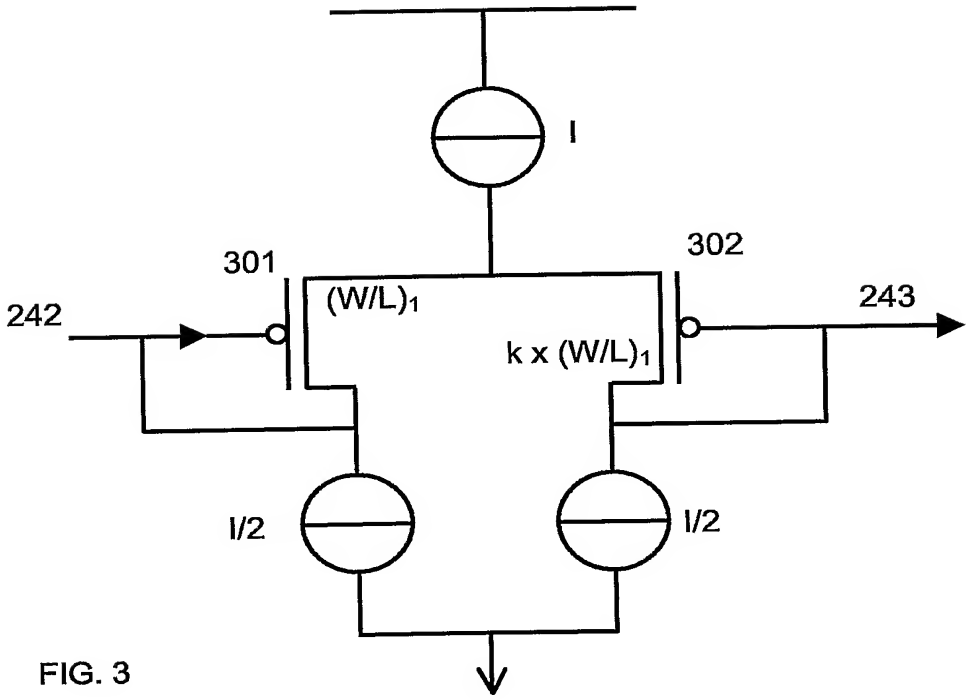
I
301
302
242
(W/L)1
243
k x (W/L)1
I/2
I/2

FIG. 3

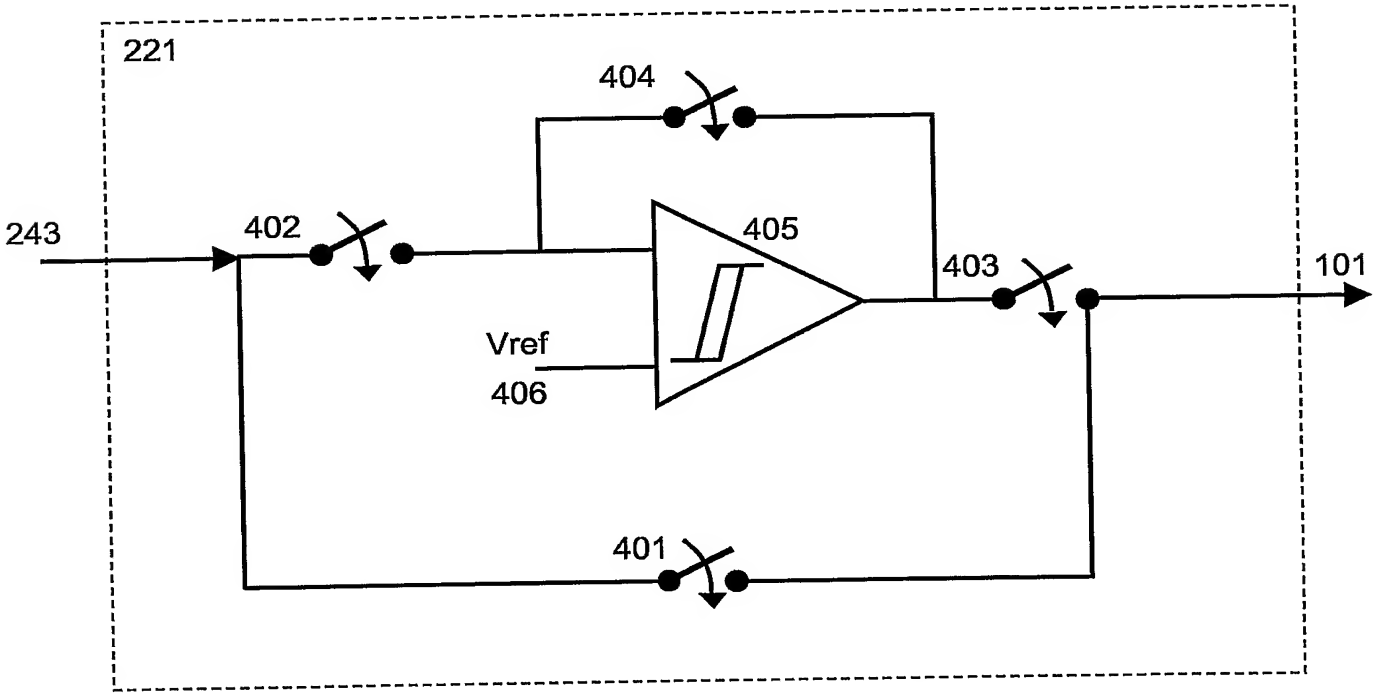
221
404
243
402
405
403
101
Vref
406
401

FIG. 4

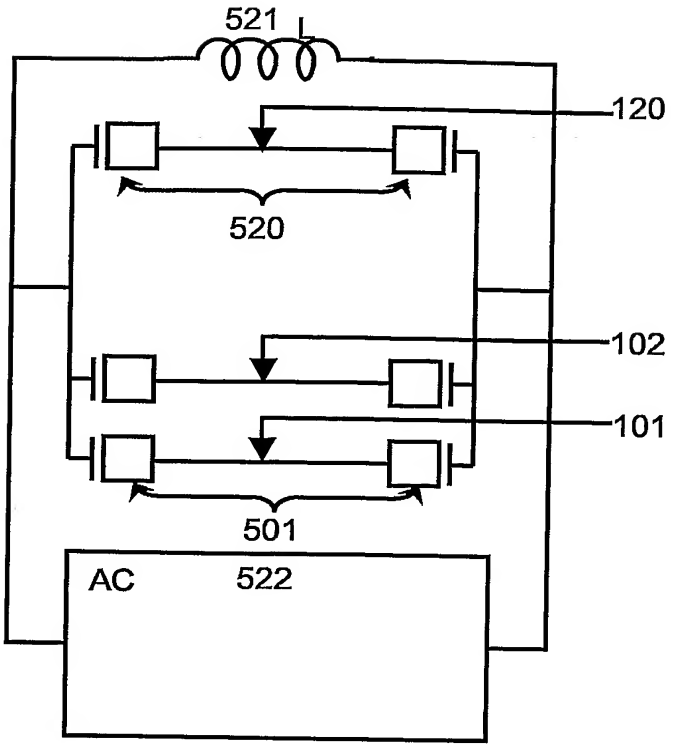
521
L
120
520
102
101
501
AC
522

FIG. 5

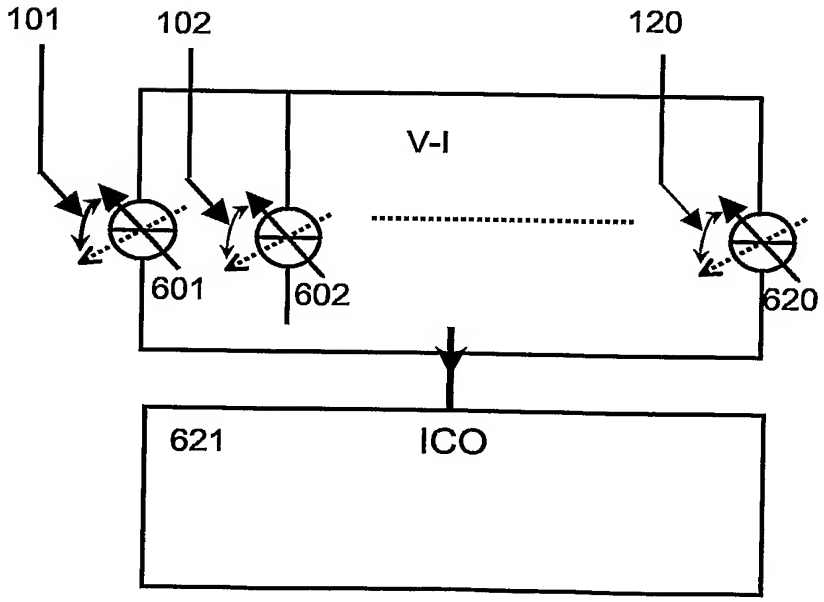
101
102
120
V-I
601
602
620
621
ICO

FIG. 6

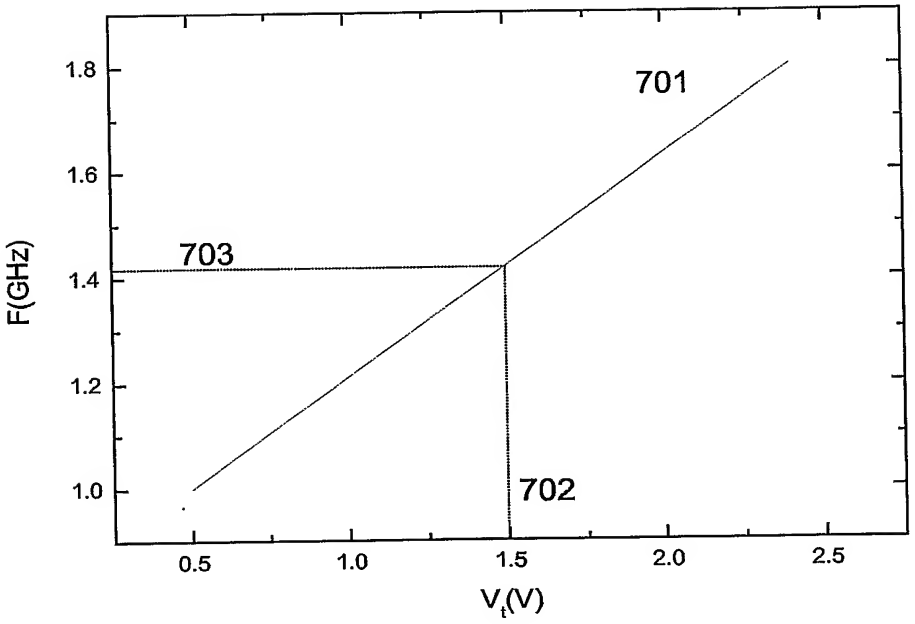
F(GHz)
1.8
1.6
1.4
1.2
1.0
701
703
702
0.5
1.0
1.5
2.0
2.5
V_t(V)

FIG. 7

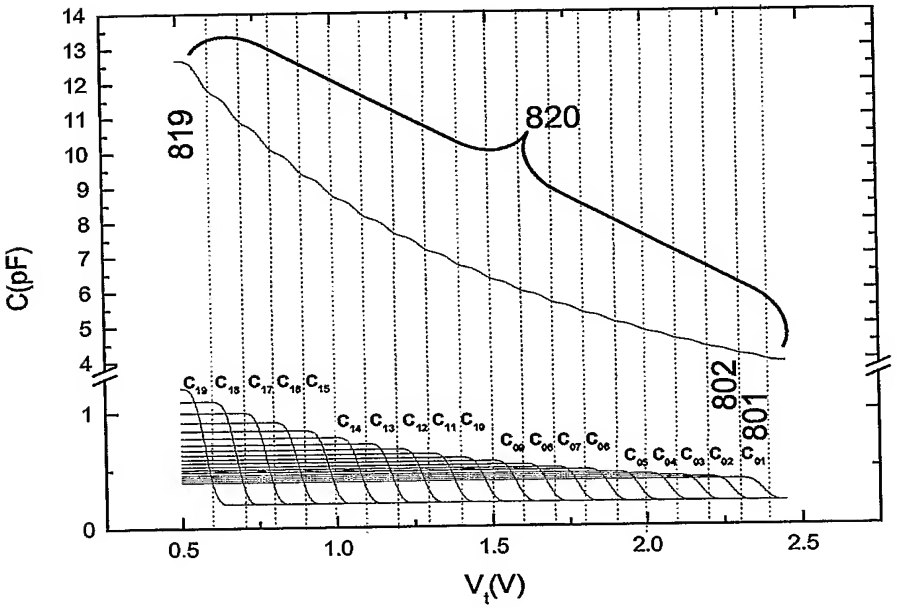
C(pF)
14
13
12
11
10
9
8
7
6
5
4
1
0
819
820
802
801
C19 C18 C17 C16 C15
C14 C13 C12 C11 C10
C09 C08 C07 C06
C05 C04 C03 C02 C01
0.5
1.0
1.5
2.0
2.5
V_t(V)

FIG. 8

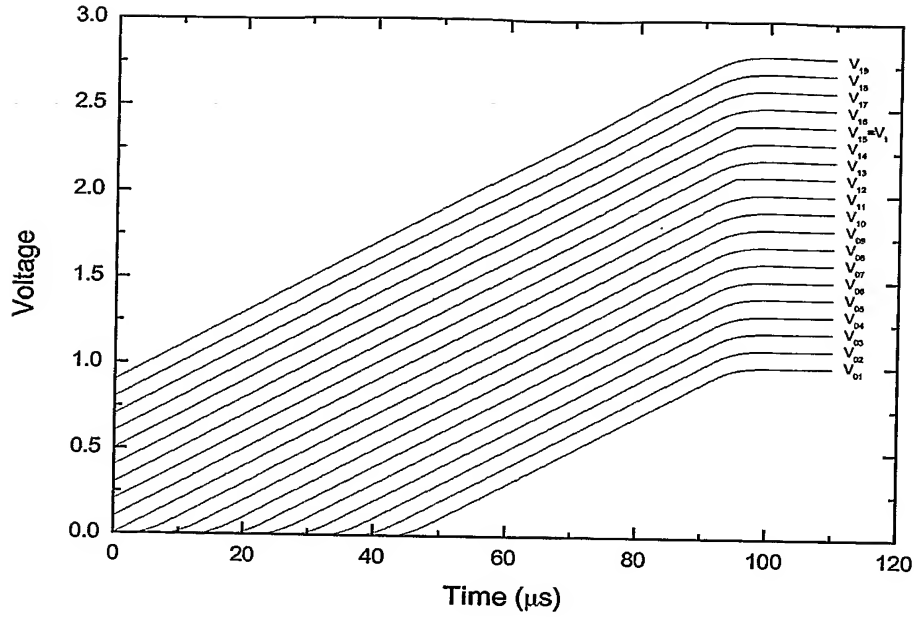
3.0
2.5
2.0
1.5
1.0
0.5
0.0
Voltage
0
20
40
60
80
100
120
Time (μs)

FIG. 9

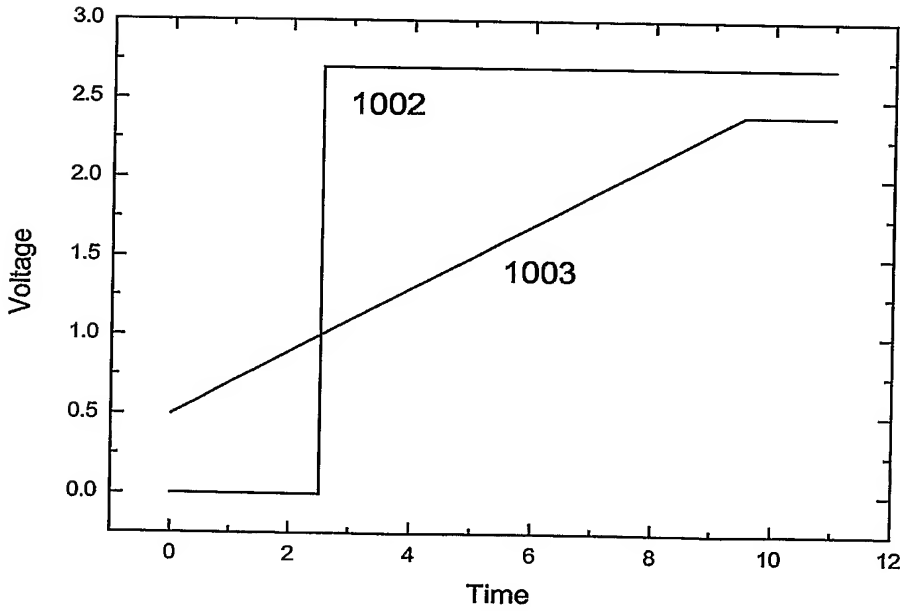
3.0
2.5
2.0
1.5
1.0
0.5
0.0
Voltage
1002
1003
0
2
4
6
8
10
12
Time

FIG. 10

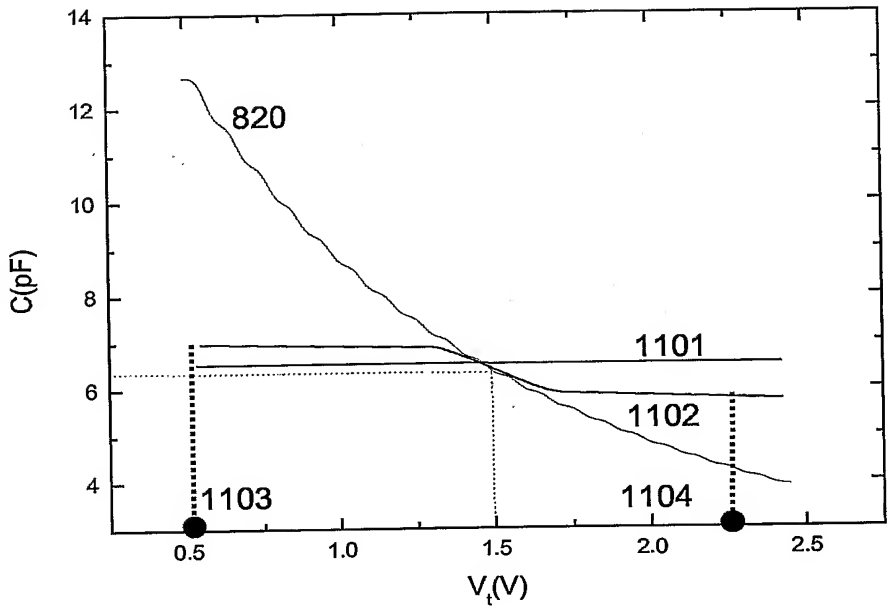
14
12
10
8
6
4
C(pF)
820
1101
1102
1103
1104
0.5
1.0
1.5
2.0
2.5
V_t(V)

FIG. 11

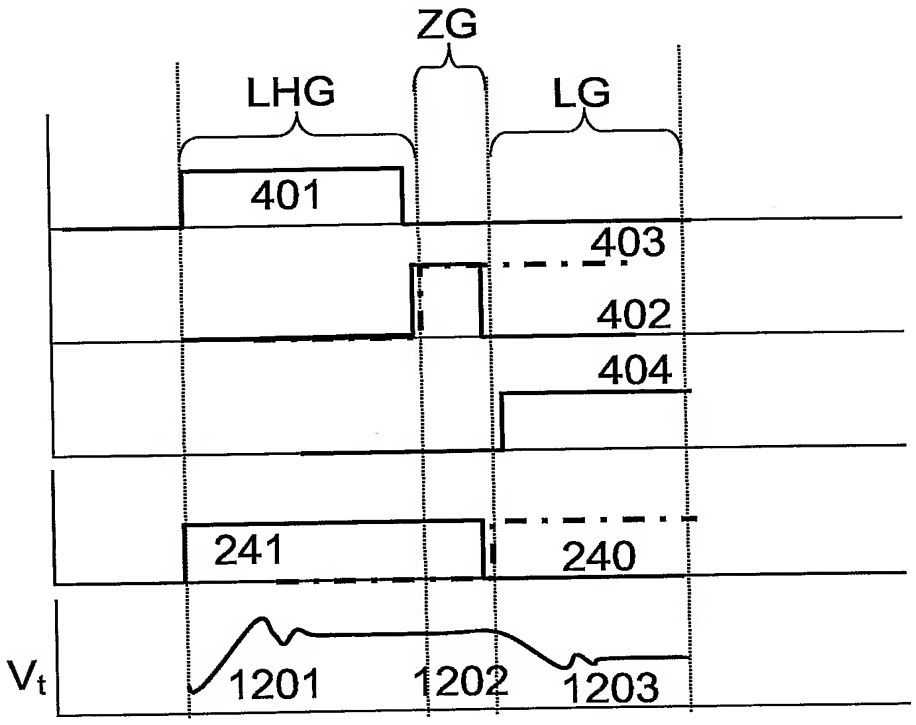
ZG
LHG
LG
401
403
402
404
241
240
V_t
1201
1202
1203

FIG. 12